Sub: MPP

S.E.(EXTC) 2016-17

Additional Questions and Answers.

Q1. Give the functions of microprocessor.

Soln. 1. To generate all system timing signals and synchronize the transfer of data between memory,I/O and itself.

2. It also recognizes ,decodes, and executes program instructions fetched from the memory unit.

Q2. Give the functions of BIU(Bus Interface Unit) and EU(Execution Unit) in the microprocessor.

Soln. 1. The BIU generates the memory and I/O addresses for the transfer of data between the outside world (outside CPU) and EU.

2. The EU receives program instruction codes and data from the BIU,executes these instructions,and stores the result in the general data registers.

Q3. What happens when the 8086 is first started?

Soln. 1. The BIU outputs the contents of the instruction pointer register(IP) onto the address bus ,causing the selected byte or word to be read into the BIU.

2. IP register is incremented by 1 to prepare for the next instruction fetch.

3. Once inside the BIU, the instruction is passed to the *queue*. The queue is a First in first out storage register similar to a "pipeline".

4. Assuming that the queue is initially empty, the EU immediately draws the instruction from the queue and begins execution.
5. While the EU is executing the instruction , the BIU proceeds to fetch a new instruction. Depending on the execution time of the first instruction, the BIU may fill the queue with several new instructions before the EU is ready to draw its next instruction.

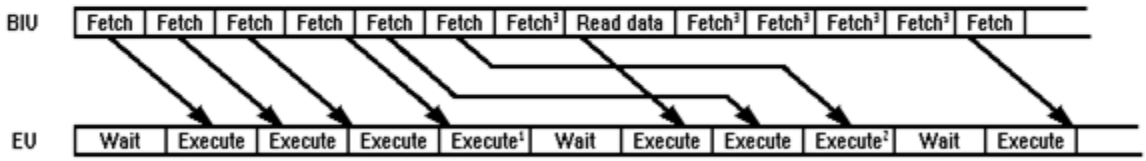
Q4. Give the three conditions for which the execution unit will go into the "wait" mode.

Soln. 1. **Instruction requiring access to memory location , not in the queue.**The BIU must suspend fetching instructions and output the address of this memory location. After waiting for memory access ,the EU can resume executing the instruction codes from the queue(and the BIU can resume filling the queue).

2. **Instruction to be executed is a 'jump' instruction.** In this case the control is to be transferred to a new (nonsequential) address. Hence the queue will be holding the "wrong" instruction codes. Hence the "wrong" data bytes must be discarded . The EU must wait while the instruction at the jump address is fetched.
3. **Instructions which are slow to execute.** E.g. the instruction AAM(ASCII adjust for multiplication) requires 83 clock cycles to complete. At four clock cycles per instruction fetch , the queue will be completely filled during the execution of this single instruction. The BIU will thus have to

wait for the EU to pull two bytes from the queue before resuming the fetch cycle.

FETCH AND EXECUTE CYCLE



[1]This instruction requires a request for data not in the queue
[2]Jump instruction occurs
[3]These bytes are discarded

INSTRUCTION PIPELINE