Sub: MPP

S.E.(EXTC) 2016-17

Questions and Answers.

Q5. What are the advantages of memory segmentation of 8086? -----5 marks

Soln. 1. The code, data, and other form of data can be stored in separate segments.

2. One program can work on several different sets of data because of separate data and code segments.
3. Programs that reference logical addresses only can be loaded and run anywhere in the memory. This is because the logical addresses always range from 0000 to FFFFH, independent of the code segment base.
4. Programs can be relocatable, means that they will run at any location in memory. Only the requirements for these relocatable programs is that , physical addresses are not referred and no changes to the segment registers are allowed.

Q6. Explain the significance of RESET and READY signal in 8086.- 5 marks

Soln. RESET: This input (active high) causes the 8086 to terminate its present activity and perform a reset sequence. The status of the "old" job is lost. RESET is normally used when first starting the system or after a system crash.

READY: This signal is an input to the 8086, provided by a slow memory device that cannot supply data fast as required with normal CPU timing.

If this input is found low (“not ready”) , then the 8086 “waits” for the slow device. This repeats until the READY input is found high.

Q7. Describe the functions of the following pins of 8086 .-------10 marks

1) NMI 2) READY 3) ALE 4) QS0 and QS1 5) S0,S1,S2

Soln. 1. NMI : It is an hardware initiated interrupt request. It is rising edge triggered. It is a non-maskable interrupt and will always be serviced. When NMI is active, control automatically transfers to the address stored in locations 00008-0000BH.

2. READY: This signal is an input to the 8086, provided by a slow memory device that cannot supply data fast as required with normal CPU timing. If this input is found low (“not ready”) , then the 8086 “waits” for the slow device. This repeats until the READY input is found high.

3. ALE : (Address Latch Enable): This is an output from 8086. An output on this pin can be used to demultiplex the address, data and status lines on AD0-AD15, A16/S3-A19/S6, and $\overline{BHE}$ / S7. When the microprocessor starts executing instructions, initially the ALE is pulsed high, so that the 20 bit address is strobed into the latch.

4. QS0 and QS1: These two pins are intended for coprocessors .They allow the coprocessor to track the progress of an instruction through the queue and help it to determine when to access the bus for the escape opcode and operand.

QS1	QS0	Current Instruction
0	0	No operation
0	1	First byte of opcode from queue
1	0	Empty the queue(transfer of control)
1	1	Next byte from queue

5. $\overline{S0}$,$\overline{S1}$ and $\overline{S2}$: These three output pins are intended for the 8288 bus controller. They encode the control bus signals when the maximum mode of operation is selected.

$\overline{S2}$	$\overline{S1}$	$\overline{S0}$	Processor state	8288 active output
0	0	0	Interrupt acknowledge	$\overline{INTA}$
0	0	1	Read I/O port	$\overline{IORC}$
0	1	0	Write I/O port	$\overline{IOWC}$
0	1	1	Halt	None
1	0	0	Code access	$\overline{MRDC}$
1	0	1	Read memory	$\overline{MRDC}$
1	1	0	Write memory	$\overline{MWTC}$
1	1	1	Passive	None

Q8. Describe the function of the following pins of 8086 in maximum mode of Operation. 1) TEST 2) $\overline{RQ/GT0}$ 3) $\overline{RQ/GT1}$ 4) QS0 and QS1 5) $\overline{S0}$, $\overline{S1}$, $\overline{S2}$ ---------- 10 marks

Soln. 1. $\overline{TEST}$: this input is used together with the WAIT instruction. If the $\overline{TEST}$ input is high when the WAIT instruction is encountered , execution of the program is suspended and the CPU enters an idle mode. Only when the $\overline{TEST}$ returns low , the CPU will resume execution (with the instruction following WAIT). This input is driven by 8087.

2. $\overline{RQ0/GT0}$ **and**

3. $\overline{RQ1/GT1}$ **:** These two pins are bidirectional, allowing a co-processor to request control of the system buses(similar to the minimum mode's HOLD request). The 8086 responds by disconnecting itself from the system buses and giving an acknowledgement on $\overline{RQ/GT}$. A direct memory access now occurs by the coprocessor. When finished, the coprocessor again pulses the $\overline{RQ/GT}$ line and the CPU reclaims the system buses. $\overline{RQ0/GT0}$ has higher priority.

4. **QS0 and QS1:** These two pins are intended for coprocessors .They allow the coprocessor to track the progress of an instruction through the queue and help it to determine when to access the bus for the escape opcode and operand.

QS1	QS0	Current Instruction
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$\overline{S2}$	$\overline{S1}$	$\overline{S0}$	Processor state	8288 active output
0	0	0	Interrupt acknowledge	$\overline{INTA}$
0	0	1	Read I/O port	$\overline{IORC}$
0	1	0	Write I/O port	$\overline{IOWC}$
0	1	1	Halt	None
1	0	0	Code access	$\overline{MRDC}$
1	0	1	Read memory	$\overline{MRDC}$
1	1	0	Write memory	$\overline{MWTC}$
1	1	1	Passive	None